# ABSTRACT OF THE DISCLOSURE

A timing debug tool for an IC that enables varying the skew of selected edges of a primary clock signal for a controllable number of clock cycles. The debug tool enables identification, isolation and analysis of timing problems on the IC. An IC including programmable clock skew logic that applies a programmed skew amount to selected edges of a clock signal. A debug system including clock control logic further including a delay block and test logic. The delay block delays a selected number of transitions of a first clock signal to provide a second clock signal, where each selected transition of the second clock signal is delayed, based on a sync signal, by either one of a default skew amount and a programmed skew amount. The test logic enables dynamic control of the sync signal and dynamic programming of the selected skew amount.